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L14	l13 and data same processor	20	L14
L13	L12 and (disconnect or unconnect)	33	L13
L12	L11 and second	183	L12
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L10	L8 and paths	209	L10
L9	L8 and first and second near paths	0	L9
L8	L7 and (ic or "integrated circuit")	1238	L8
L7	(electronic near money or electronic near purse)	3018	L7
L6	L5 and (disconnected or unconnected)	14	L6
L5	L4 and paths	108	L5
L4	L3 and (ic or "integrated near circuit")	532	L4
L3	L1 and communication	1279	L3
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each group facilitates the multiprocessor operation and is associated with a processor (1-4) of FIG. 13. Each of the four groups includes one base pointer register, effective address register, instruction pointer register, top of stack register, stack pointer register, return pointer register, instruction register, CRC register, next register, and a carry flag. Each related group of registers corresponds to one of the four processors. Each processor executes instructions in minor cycles, each minor cycle consisting of four clock cycles. During the first clock cycle a processor will gate the appropriate registers onto the ABUS, BBUS and CBUS. In the next clock cycle the ALUs will be active generating data from their inputs of the ABUS, BBUS and CBUS. Memory or I/O will be active during the third clock cycle, with the address coming from the ALU 102a and data either being sourced by memory or the ALU 102b. The fourth and final clock cycle will gate the results from memory or the ALU 102b into the appropriate register via the DBUS.

Detailed Description Text (153):
A processor can be viewed as a wave of data propagating through the sequence described above. At each step the intermediate results are clocked into a set of pipeline registers. By using these pipeline registers it is possible to separate the individual steps in the sequence and therefore have four steps executing simultaneously. The four processors can operate without interfering with one another even though they share the ALUs, memory, I/O and many control circuits.

Detailed Description Text (155):
The count (e.g., 3 bits) in a counter and the instruction (e.g., 12 bits) in its associated instruction register from a 15 bit input to the PLA 136. These 15 bit inputs from each of the respective four sets of count registers and four sets of instruction registers are sequentially coupled to the PLA 136 as will be described. The output of the PLA controls the operation of the processors. More specifically: lines 213 control data flow on the ABUS, BBUS and CBUS; lines 214 control the ALU 102; lines 215 control the memory; (and, as will be described later I/O operation of subsections 107, 108, 109 and 220) and lines 216 control data flow on the DBUS. The specific outputs provided by the PLA 136 for a given instruction is best understood from the instructions set, set forth later in this application. The action taken by the processors to execute each of the instructions is described with the instruction set.

Detailed Description Text (156):
The outputs from the PLA on lines 213 are coded directly to the devices controlling data flow on the ABUS, BBUS, and CBUS. The signals controlling the ALU are coupled through a one clock phase delay register 217 before being coupled to the ALU via the lines 214. Since all the registers 217 are clocked at the same rate, the register 217 performs delay functions as will be described. Those signals from the PLA 136 used for memory control are coupled through two stages of delay registers 217 before being coupled to the memory, thus the signals on lines 215 are delayed for two clock phases related to the signals on lines 213. The control signals for the DBUS after leaving the PLA 136 are coupled through 3 sets of delay registers 217 before being coupled to the lines 216 and therefore are delayed three clock phases related to those on lines 213. The registers 217 are clocked at a 6 mHz rate, thus when the PLA 136 provides output control signals for a given instruction (e.g., contents of instruction register 125a) the control signals during a first phase are coupled to lines 213, during a second clock phase, lines 214; during a third clock phase, 215; and during a fourth clock phase to lines 216. During the first clock phase of each instruction cycle, the contents of the counter 137a and the instruction register 125a are coupled to the PLA 136. During the second clock phase, the contents of the counter 137b and instruction register 125b are coupled to the PLA 136 and so on for the third and fourth clock phases.

Detailed Description Text (157):
Assume now that instructions have been loaded into the instruction registers 125a through 125d and the counters 137a through 137d have been loaded with the

corresponding binary counts for the minor cycles needed to perform each of the instructions. For example, assume that register 125a is loaded with a CALL instruction and that 010 has been loaded into counter 137a. During a first instruction minor cycle, 010 and the 12 bit instruction for CALL are coupled to the PLA 136. From this 15 bit input PLA 136 provides at its output all the control signals needed to complete the first minor cycle of the CALL instruction (e.g., four clock phases) for the ABUS, BBUS CBUS, the ALU, the memory and the DBUS. Since the system uses pipelining multiprocessing, the control signals on lines 213 used to carry out the first clock phase of the CALL instruction which is the inputs to the ALUs. (During this first clock phase the other control lines are controlling the ALU, the memory and the DBUS of other processors, for different instructions in the pipelines.) During phase 2, the count in counter for 137b and the instruction in register 125b are coupled to the PLA 136. During phase 2, the signals on lines 213 now control the ABUS, BBUS and CBUS inputs to the ALUs for the second processor to carry out the instruction contained in register 125b. During this second clock phase, the signals on lines 214 control the first processor and the ALU to perform the functions needed to carry out the second clock phase of the CALL instruction contained in register 125a. (Note a delay equal to one phase was provided by register 217). Similarly, during the third phase, the signals on lines 213 control the ABUS, BBUS, and CBUS for the third processor to carry out the instruction contained in register 125c; the signals on lines 214 control the ALU to carry out the instruction contained in register 125b, and the signals on lines 215 control the memory to carry out the instructions in register 125a for the first processor. And, finally, during the fourth clock phase, the instruction from register 125d, along with the count in counter 137d are coupled to the PLA 136. The signals on lines 213 control the ABUS, BBUS and CBUS to carry out the instruction contained within register 125d fourth processor; the signals on lines 214 control the ALU to carry out the instruction in register 125c for the third processor; the signals on lines 215 control the memory to carry out the instruction in register 125b for the second processor; and the signals on lines 216 control the DBUS to carry out the instruction in register 125a for the first processor.

Detailed Description Text (158):
After four cycles of the 16 mHz clock the count in register 137a decrements to 001. Each register is decremented on the clock cycle following the use of the contents of the counters contained by the PLA 136. The input to the PLA 136 thus changes even though the instruction within register 125a is the same. This allows the PLA 136 to provide new output signals needed for the second minor cycle of the CALL instruction. These control signals are rippled through the control through the control lines 213, 214, 215 and 216 as described above. When the count in a counter reaches 000, this is interpreted as an instruction fetch for its associated processor.

Detailed Description Text (159):
Therefore, each of the four processors may simultaneously execute an instruction where each of the instructions has a different number of cycles. The control signals reaching the imaginary line 219 for any given clock cycle represent control signals for four different instructions and for four different processors. For example, the control signals associated with the first processor during a first cycle appear on lines 213; during a second cycle on lines 214; during a third cycle on lines 215; and during a fourth cycle on lines 216. The control signals needed by the second processor follow behind; those needed by the third and fourth processors following behind those used by the second processor.

Detailed Description Text (161):
During a first phase, signals previously stored in the group 1 registers (e.g., two of them) are gated from the registers onto the ABUS, BBUS and CBUS. While this is occurring, signals associated with the group 2 registers are gated from the registers 141, 142, 143 into the ALU 102a and 102b. This is shown in FIG. 13 as processor 2 under the first phase column. Simultaneous signals are gated from

registers 145a and 145b into the memory for group 3 registers for processor 3. And, finally, during this first phase, signals associated with the group 4 registers are gated from registers 146 onto the DBUS. During the second phase, signals associated with a group 1 registers are coupled from the ALU to registers 145. The data associated with group 2 registers are coupled to memory. The data associated with the group 3 registers is coupled from the register 146 onto the DBUS. Those associated with the group 4 registers are gated onto the ABUS, BBUS and CBUS. And, similarly, during the third and fourth phase of each instruction cycle, this pipelining continues as shown in FIG. 13, thus effectively providing four processors.

Detailed Description Text (167):
Referring to FIG. 14 the register 142 is illustrated with four bits of the register containing data D0 through D3. If the ALU is commanded to encode this data, the resultant six bits will be coupled into the latch register 145b. To obtain the conversion shown in FIG. 9, the D.sub.0 bit is directly coupled to the first stage of register 145b and becomes E.sub.0, the encoded bit. Also, the bit D.sub.3 is directly coupled into the register and becomes E.sub.5. Each of the remaining bits E.sub.1 through E.sub.4 are provided by the logic circuits 153 through 150, respectively. Each of these logic circuits are coupled to receive D.sub.0, D.sub.1, D.sub.2 and D.sub.3. Each logic circuit contains ordinary gates which implement the equation shown within its respectibe block. These equations are shown in standard "C" language ("&"=logical AND, "!"=logical NOT, and ".vertline."=logical OR.) These equations can be implemented with ordinary gates.

Detailed Description Text (182):
The output of the multiplier 178 in each of the subsection is coupled to an 8 bit counter 179. The counter can be initially loaded from a counter load register 180 from the data bus of the processors. This register can, for example, receive data from a program. The count in the counter is coupled to a register 181 and to a comparator 182. The comparator 182 also senses the 8 bits in a register 183. The contents of this register are also loaded from the data bus of the processors. When a match between the contents in the counter and the contents of register 183 is detected by comparator 182; the comparator provides an event signal to the state machine of FIG. 19 (input to multiplexers 190 and 191). The contents of the counter 179 can be latched into register 181 upon receipt of a signal from the state machine (output of the execution register 198 of FIG. 19). The same execution register 198 can cause the counter 179 to be loaded from register 180. When the counter reaches a full count (terminal count) a signal is coupled to the state machine of FIG. 19 (input to multiplexers 190 and 191).

Detailed Description Text (185):
The multiplexers 190 and 191 both receive the terminal count signal from counter 179 of FIG. 18, the compare signal from comparator 182, the ramp start signal from the ramp generator 200 of FIG. 20, and the transition A and B signals from the transition detectors 171 and 172, respectively of FIG. 17. The one output from each of the multiplexers 190 and 191 is coupled to an OR gate 188. This OR gate is biased in that if an output occurs simultaneously from both multiplexers 190 and 191, priority is given to multiplexer 190. The output of the multiplexer 190 controls the multiplexer 187 with the signal identified as "which event". This signal is also stored in the 3.times.3 first-in, first-out (FIFO) buffer 199. This signal indicates which MUX 190 or 191 has received an event and this data is stored along with the inputs to Pin A and Pin B (FIG. 17) in the FIFO 199.

Detailed Description Text (191):
Referring first to FIG. 20, the I/O subsystem includes a ramp generator 200 which continually generates ramps of a known period. The output of the ramp generator is buffered through buffer 201 and selected by switch 202. The switch, as will be described, is selected at some count (time) following the start of each ramp, thereby coupling the same potential to the capacitor 203. This capacitor becomes

charged and potential is coupled through buffer 204 to Pin A when the switch 175 is closed (Switch 175 is shown in FIG. 17.) The switch 202, capacitor 203, and buffer 204 act as a sample and hold means.

Detailed Description Text (197):
Referring to FIG. 23 during the hunt mode, an I/O subsection is hunting for data. During this mode, the rate multipler provides a frequency (f.sub.0) to the counter 179 and a number is loaded into register 183 from the MBUS. Matches occur and are detected by comparator 182 at a frequency corresponding to the expected incoming data rate. Specifically, the terminal count of counter 179 is synchronized to the transitions. As indicated by the dotted line 201, the processor continually searches for transitions from the transition detectors 171 and 172 of FIG. 17. When transitions occur, the processor determines whether the transitions occurred before or after the terminal count and then adjusts the frequency (f.sub.0) until the terminal count occurs at the same time that the transitions are detected. This frequency is the shifting rate for the shift register 206. (The steps performed by the processor are shown in FIG. 23 as blocks 210 and 211.) The number loaded into register 183 provides a phase shift between the time at which transitions occur and the ideal time to shift data in the register 206. This prevents the shifting of data during transitions. Note counter 179 is reloaded (e.g., all zeroes) each time it reaches a terminal count.

Detailed Description Text (199):
The comparator output is used as a shift rate for a six bit shift register 206. During the hunt mode, the data from Pin B is continually shifted through register 206. The preamble to a packet as shown in FIG. 9 (010101-bit synch) is shifted along the shift register 206 and the shifting rate adjusted so that synchronization/lock occurs. When the packet beginning flag appears (nibble synch-101010) the last two stages of the register 206 will contain ones and this will be detected by the AND gate 207. A binary one at the output of gate 207 ends the hunt mode and provides the nibble synchronization. When this occurs, the data is clocked out of the shift register (6 bits) into a data latch 235 and from there the data can be clocked into the processor and converted into 4 bit nibbles. Another circuit means is present to detect all zeroes in the shift register 206. When this occurs, the processor and shift register return to the hunt mode. the number loaded into register 183 provides a phase shift between the time at which transitions occur and the ideal time to shift data in and out of the register 206. This prevents the shifting of data during transitions.

Detailed Description Text (217):
The network uses a carrier sense multiple access method of resolving contention for the communications channel. When a cell is ready to transmit it first listens to the communications channel. If it hears another cell transmitting, it waits for a clear channel. Once it detects a clear channel, a cell may delay before transmitting. The method of determining that delay is determined by the contention algorithm.

Detailed Description Text (220):
A packet from a group announcer to a set of group listeners will cause each of those listeners to send an acknowledgement to the announcer. Without a method of arbitrating contention among those acknowledgements, they will always collide. To avoid this problem, a built in reservation system for group acknowledgements is used. A listener cell uses its group member number to determine which slot to use for its acknowledgement. Group member 5 will transmit its acknowledgement in the 5th free slot following reception of the original packet. The result is that group member 1 will transmit its acknwledgement in the first slot following the original packet. Group member two will transmit its acknowledgement in the first slot following first group member's acknowledgement. This process continues until the last group member has replied to the original packet. If a group member does not reply and thus leaves its reply slot empty, the next group member replies in the

next slot.

Detailed Description Text (243):
When a control device wishes to communicate with a cell, it opens communications by sending a packet with a connect command in the link control field. That command initializes the sequence numbers. After receipt of that command, the cell will not accept messages addressed to it (via cell address) by another control device until the conversation ends. The conversation ends when the control device sends the cell a disconnect command.

Detailed Description Text (259):
When a packet is received, the processor calculated a CRC for the received packet by first placing its stored CRC preset field in its CRC register and then computing the packet CRC (again, the contention timer field is not used). If the newly computed CRC field does not match the field in the packet, it is assumed that the packet has been improperly transmitted or that the transmitted packet, if correct 14 received, has a different system ID and thus should be discarded.

Detailed Description Text (610):
Function: report the address list in the first probe packet received by the destination Cell.

Detailed Description Paragraph Table (1):
______________________________________ FIG. 12 IDENTIFICATION
______________________________________ ip instruction pointer (14 bits) 120 (fixed range of 0000-3FFF) (not accessible to ROM based programs) ir instruction register (12 bits) 125 (not accessible to ROM based programs) bp base page pointer (14 bits) 118 (fixed range of 8000-FFFF) (write only) ea effective address pointer (16 bits) 119 (not accessible to ROM based programs) sp data stack pointer (8 bits) 123 (positive offset from bp, grows down) rp return stack pointer (8 bits) (positive offset from bp, grows up) 124 tos top of data stack (8 bits) 122 next item below top of data stack (8 bits) 131 crc used as scratch or in 130 CRC calculations (8 bits) flags carry flags, (1 bit) 129 processor ID (2 bits)

____

Detailed Description Paragraph Table (6):
______________________________________ ARQ Protocol Commands INFO Information Packet (requires acknowledgement) ACK Acknowledgement Only Packet (does not require acknowledgement) Connection Control Commands CONN Connect DISC Disconnect SI Set Initialization XND Exchange Network Data Replies to Connection Control Commands CMDR Command reject RD Request Disconnect RI Request Initialization UA Unnumbered Acknowledge ______________________________________ Only packets with the ACK and INFO commands use sequence numbering. The INFO packets have two sequence numbers, a transmit sequence number and the sequence number of the last packet received. ACK packets have both sequence number fields but the transmit sequence number is ignored by the destination.

Detailed Description Paragraph Table (7):
____ __ Primary Secondary Command Response Description
____ INFO Information: valid only in connect state. INFO Information: valid only in connect state. ACK Acknowledgement: use sequence numbers in packet but do not update receive sequence number. CMDR Command reject: sent only by Secondary in Connect State. Rebuild pckt and send it again. RI Request initialization: init secondary. disconnect secondary. RD Request Disconnect: disconnect the secondary. DM Secondary is in the Disconnect state ACK Acknowledgement CMDR Command reject: sent only by secondary in connect state. Rebuild pckt and send it again. RI Request initialization: init secondary. disconnect secondary. Connect secondary. DM Disconnect Mode: Secondary is in the disconnect state. CONN Connect UA Unnumbered

ACK: CMDR Command reject: sent only by Secondary in connect state retry CONN: RI Request initialization: init secondary. disconnect secondary, connect secondary. RD Request disconnect: send DISC. DISC Disconnect UA Unnumbered ACK CMDR Command reject: sent only by secondary in connect state. Retry DISC. SI Set Initialization CMDR Command reject: Sent only by secondary in Connect State. Retry SI. UA Unnumbered ACK. XND Exchange ID & Network data: This command is sent only in when the primary is in the disconnect state. XND Exchange ID & Network data: The secondary sends an XND response only if it is in the disconnect state. If it receives an XND while in any other state, the secondary responds with CMDR. CMDR Command reject: sent only by secondary in connect state. Disconnect secondary; then try XND again.

Detailed Description Paragraph Table (8):

State

Event Action Next State

PRIMARY

STATION CONNECTION STATES 0. Start Power Up Initialize 4. Wait Init 1. Disconnect Connect Request Send CONN 2. Wait Connect 1. Disconnect Fatal Error or RI Send SI 4. Wait Init 1. Disconnect XND Process XND 1. Disconnect 1. Disconnect INFO, ACK Retry DISC 1. Disconnect 1. Disconnect UA, DM Ignore 1. Disconnect 1. Disconnect RD, CMDR Retry DISC 1. Disconnect 2. Wait Connect UA Reset Seq Nums 3. Connect 2. Wait Connect Fatal Error or RI Send SI 4. Wait Init 2. Wait Connect Nonfatal error, RD, or CMDR Send DISC 5. Wait Disc. 2. Wait connect INFO, ACK Send DISC 5. Wait Disc. 2. Wait Connect DM Retry CONN 3. Wait Connect 2. Wait Connect XND Send DISC 5. Wait Disc. 2. Wait Connect Time out Retry CONN 2. Wait Connect 3. Connect Fatal Error or RI Send SI 4. Wait Init. 3. Connect Nonfatal error, RD, or disc. Send DISC 5. Wait Disc. request 3. Connect DM Send DISC 1. Disconnect 3. Connect CMDR, INFO,ACK ARQ Processing 3. Connect 3. Connect XND Send DISC 5. Wait Disc. 3. Connect UA Send DISC 5. Wait Disc. 4. Wait Init UA received Send DISC 5. Wait Disc. 4. Wait Init CMDR received Retry SI 4. Wait Init 4. Wait Init INFO, ACK Retry SI 4. Wait Init 4. Wait Init RD, DM,RI,XND Retry SI 4. Wait Init 4. Wait Init Time out Retry SI 4. Wait Init 5. Wait disc UA, DM 1. Disconnect 5. Wait disc RI Send SI 4. Wait Init 5. Wait disc Fatal error Send SI 4. Wait Init 5. Wait disc CMDR, RD, XND Retry DISC 5. Wait Disc. 5. Wait Disc INFO, ACK Retry DISC 5. Wait Disc. 5. Wait Disc Time out Retry DISC 5. Wait Disc. SECONDARY STATION CONNECTION STATES 0 Start Power Up Initialization 3. Initialize 1. Disconnect CONN received Send UA 2. Connect 1. Disconnect SI received Initialization 3. Initialize Send UA 1. Disconnect Fatal Error Send RI 4. Wait Init. 1. Disconnect XND Send XND 1. Disconnect 1. Disconnect INFO, ACK Retry DM 1. Disconnect 1. Disconnect DISC Retry DM 1. Disconnect 2. Connect SI received Initialization 3. Initialize Send UA 2. Connect DISC received Send UA 1. Disconnect 2. Connect Fatal Error Send RI 4. Wait Init. 2. Connect Nonfatal error Send RD 5. error 2. Connect INFO, ACK ARQ Processing 2. Connect 2. Connect CONN Retry UA 2. Connect 2. Connect XND Send RD 5. Error 3. Initialize DISC received Send UA 1. Disconnect 3. Initialize INFO, ACK,CONN Retry RI 3. Initialize 3. Initialize SI Retry UA 3. Initialize 3. Initialize XND Retry RD 3. Initialize 4. Wait Init. SI received Initialization 3. Initialize Send UA 4. Wait Init INFO, ACK Retry RI 4. Wait Init 4. Wait Init DISC, XND, CONN Retry RI 4. Wait Init 5. Error DISC received Send UA 1. Disconnect 5. Error SI received Initialization 3. Initialize Send UA 5. Error INFO, ACK Retry RD 5. Error CONN, XND

Detailed Description Paragraph Table (9):

APPENDIX C APPLICATIONS CATEGORY SUBCATEGORY APPLICATION

General

Sensing Functions Usage Communication Functions Control Functions Agriculture Crop Management Crop Sensor/Comm Irrigation Ctrl/Comm Land Leveler Sensor Comm Pest Sensor/Comm (with cell IDs identifying animals) Livestock Detector/Tracker Feed

Sense/Ctrl/Comm Milker Sense/Ctrl/Comm Weight Sensor/Comm Herder Signal Device Commercial Banking ATM Card Electronic Money Commercial Cash Register Sense/Ctrl/Comm Elevator Sense/Ctrl/Comm Slot Machine Sense/Ctrl/Comm Vending Machine Sense/Ctrl/Comm Commercial, Misc Diaper Sensor/Comm Pager Ctrl/Comm Protechnics, Sensor Ctrl Stamp I.D. Watch Ctrl/ Construction Decay Sensor/Comm Post Sensor/Comm Energy Management Sensor Sense/Comm Thermostat Ctrl/Comm Utility Sensor/Comm Vent Ctrl/Comm Security Lock Sense/Ctrl/Comm Smart Keys (Serial #) Communication Communications Cable Elimination Channel Ctrl/Comm Network Configuration Ctrl/Comm Cell to Anything Bridge Phone I.D. (Cell I.D.) Phone to Cell Bridge Telemetry Ctrl/Comm Wiring Elimination Computer Slow Data Network Network Architecture Artificial Intelligence Configuration Ctrl Copy Protection Parallel Processing Nodes Peripheral Cable Elimination Keyboard Sense/Comm Mouse Sense/Comm Wiring Elimination Develop. System Emulator Device Consumer Appliances Sensor Sense/Comm Switch Sense/Ctrl/Comm Consumer, Misc Detector/Tracker (Electronic Serial #) Low Battery Detector Smart Lottery Ticket Entertainment Amusement Park Ctrl'r Arcade Game Ctrl'r Cable TV Access Ctrl'r Cable TV Sample Ctrl'r CD Player Ctrl'r Special Effects Ctrl'r Stereo Ctrl'r TV Ctrl'r VCR Ctrl'r Home Improvement Central Clock Sys Curtain Ctrl/Comm Door Sense/Comm Garage Door Ctrl'r Intercom Intercom Ctrl'r Pool Ctrl'r Sense/Ctrl/Comm Smoke/Fire Detector Window Sense/Ctrl/Comm Pets Detector/Tracker (Electronic Serial #) Pet Ctrl/Trainer Education Education, Misc Interactive Book Sense/Ctrl/Comm Test Sense/Comm Engineering Data Acquisition DAC/ADC Instrumentation DAC/ADC Switch Sense/Ctrl/Comm Home Electrical Light Ctrl/Comm Recepticle Sense/Comm/Ctrl Switch Sense/Ctrl/Comm All forms of sensing All forms of control Energy Management Sensor Sense/Comm Thermostat Ctrl/Comm Utility Sensor/Comm Vent Ctrl/Comm Home Improvement Central Clock Sys Curtain Ctrl/Comm Door Sense/Comm Garage Door Ctrl'r Intercom Intercom Ctrl'r Pool Ctrl'r Sense/Ctrl/Comm Smoke/Fire Detector Window Sense/Ctrl/Comm Security Lock Sense/Ctrl/Comm Smart Keys (Serial #) Vibration/Motion Sense/Comm window Sense/Ctrl/Comm Sprinkler Sys Timer Ctrl/Comm Valve Ctrl/Comm Wetness Sense/Ctrl Industrial Energy Management Sensor Sense/Comm Thermostat Ctrl/Comm Utility Sensor/Comm Vent Ctrl/Comm Industrial Equipment Oil Drill Sensor/Ctrl/Comm Power Load Sense/Ctrl/Comm Utility Sensor/Comm Security Lock Sense/Ctrl/Comm Smart Keys (Serial #) Vibration/Motion Sense/Comm Window Sense/Ctrl/Comm Security, Industrial Copy Protection Detector/Tracker (Electronic Serial #) Personnel Badge I.D. Law Security, Law Copy Protection I.D. Card (Serial #) Gun I.D. Passport (Serial #) Shoplifter Detector Manufacturing CIM Artificial Intelligence Wiring Elimination Production Ctrl Detector/Tracker (Electronic Serial #) Inventory Sense/Comm Process Ctrl LIne Balance Production Automation Production Flow/Sense Robotics Detector/Tracker (Electronic Serial #) Robot Sense/Ctrl/Comm Medical Medical, Misc Bio-Feedback Bionics Handicapped Interfaces Heart Pacer Implants Medical Alert Sense/Comm Medicine Alert Sense/Comm Patient Monitoring Personal Dispenser Ctrl/Comm Personal Monitors Prosthetics Military Military, Misc Copy Protection Damage Ctrl Sense/Comm Detector/Tracker (Electronic Serial #) Personnel Badge I.D Redundant Comm SDI Sense/Ctrl/Comm Sonna Buoy Sense/Comm Spying Sense/Ctrl/Comm Position Sense/Ctrl/Comm System Diagnostics Sense/Comm War Game Monitor/Sim Weapon Sense/Ctrl/Comm Security Lock Sense/Ctrl/Comm Smart Keys (Serial #) Vibration/Motion Sense/Comm Window Sense/Ctrl/Comm Scientific Weather/Earthquake/etc. sensor Transportation Automotive General sensing General communication General control Anti-lock Breaking Sys Complex Cable Elimination Gauge Ctrl In Dash Map/Locator Instrument Panel Ctrl License Plate I.D. & Comm Light Ctrl/Comm Regulator Sense/Comm Smart Keys (Serial #) Switch Sense/Ctrl/Comm System Diagnostics Sense/Comm Wiring Elimination Avionics Anti-lock Breaking Sys Complex Cable Elimination Gauge Ctrl Instrument Panel Ctrl Light Ctrl/Comm Regulator Sense/Comm Sensor Sense/Comm Switch Sense/Ctrl/Comm System Diagnostics Sense/Comm Wiring Elimination Transportation, Misc Emergency Locator (ELT) Sense/Comm Traffic Monitor/Ctrl Traffic Signal Sense/Ctrl/Comm Tpy/Hobby/Spo Game 3-D "Chip-Wits" Sense/Ctrl/Comm Bingo Card Sense/Comm Game sense/Ctrl/Comm Hobby Camera Sense/Ctrl/Comm Hobby Kit Sense/Ctrl/Comm Magic Equipment Sense/Ctrl/Comm Miniature Train Ctrl/Comm Remote Ctrl Sense/Ctrl/Comm Sport Emergency Locator (ELT) Sense/Comm Trap Line Sensor Sport Accessory Sense/Ctrl/Comm Toy Lego-Bot

Sense/Ctrl/Comm Media Interactive Toy Sense/Ctrl/Comm Animated Toy Sense/Ctrl/Comm

Other Reference Publication (11):
"Reverse Path Forwarding of Broadcast Packets", Communications of the ACM, vol. 31, No. 12, Dec. 1978, pp. 1040-1048, by Y. Dalai and R. Metcalfe.

Other Reference Publication (24):
"Explicit Path Routing in Communications Networks", The Proceedings of the International Conference on Computer Communication, 1976, pp. 340-342, by R. Jueneman and G. Kerr.

CLAIMS:

3. The network defined by claim 1 and a second network as defined by claim 1, said networks having different system identification numbers, and a communication means for connecting said networks and for converting one of said system identification numbers to the other of said system identification numbers.

7. A network for sensing, communicating and controlling comprising:

a plurality of cells each of said cells including (1) a unique cell identification number, (2) a processor for operating upon messages, said processor of each of said cells having access to its respective cell identification number, and (3) an input/output section for coupling messages between its respective processor and a communications medium;

grouping means for causing at least a first and second of said cells to cooperate with one another as members of a first group in the performance of a first group function, said grouping means establishing said membership in said first group by employing said cell identification numbers of said first and second cells, and by assigning said first and second cells a first group identification number and tasks needed to carry out said first group function;

said first and second cells communicating with one another over said medium by using said first group identification numbers for carrying out their respective tasks through their respective processors by operating upon messages communicated between said first and second cells;

said grouping means for causing at least a third and fourth of said cells to cooperate with one another as members of a second group in the performance of a second group function, said grouping means establishing said membership in said second group by employing said cell identification numbers of said third and fourth cells, and by assigning said third and fourth cells a second group identification number and tasks needed to carry out said second group function;

said third and fourth cells communicating with one another over said medium by using said second group identification number for carrying out their respective tasks through their respective processors by operating upon messages communicated between said third and fourth cells,

a fifth of said cells assigned the task of announcing in said first group and assigned the task of listeing in said second group,

whereby a network for sensing, communicating and controlling is realized.

8. The network defined by claim 7 wherein said first cell of said first group is assigned the task of announcing and said second cell in said first group is assigned the task of listening.

11. A network for sensing, communicating and controlling comprising:

a first programmable cell comprising a semiconductor integrated circuit having a processor and an input/output section coupled to its processor, said first cell being assigned a first system identification number and a first unique cell identification number, said first cell's processor for preparing and acting upon predetermined messages which are coupled to a communications medium through said first cell's input/output section, said first cell's input/output section being coupled to a sensing means for sensing a condition, said first cell being assigned a first group identification number;

a second programmable cell comprising a semiconductor integrated circuit having a processor and an input/output section coupled to its processor, said second cell being assigned said first system identification number and second unique cell identification number said second cell's processor for preparing and acting upon said predetermined messages and for coupling said messages through its input/output section to said medium, said second cell being coupled to control means for controlling an object, said second cell being assigned said first group number;

said first and second cells communicating with one another over said medium through their respective input/output sections by using said first system identification number, their first and second cell identification numbers and said group identification number;

whereby a sensing, communicating and control network is realized.

12. The network defined by claim 11 including a third programmable cell comprising a semiconductor integrated circuit having a processor and an I/O section coupled to its processor, said third cell being assigned said first system ID and a third unique cell ID, said third cell's processor for preparing and acting upon messages, said third cell being assigned the task of repeating said predetermined messages transmitted between said first and second cells, said third cell being assigned said first group ID.

13. The network defined by claim 11 or 12 including a fourth programmable cell comprising a semiconductor integrated circuit having a processor and an I/O section coupled to its respective processor said fourth cell being assigned said first system ID and a fourth unique cell ID, said fourth cell's processor for preparing and acting upon predetermined messages, said fourth cell being assigned said first group ID and being coupled to a second control means for controlling a second object.

14. The network defined by claim 11 wherein said cell identification numbers are used for establishing said first group.

15. The network defined by claim 14 wherein a first member number is assigned to said first programmable cell within said first group and wherein a second member number is assigned to said second programmable cell within said first group and wherein said first cell and said second cell communicate with one another after said first group is established by utilizing said first and second member numbers and said group identification number.

16. A network for sensing, communicating and controlling comprising:

at least one communications medium;

a first plurality of programmable cells coupled to said medium for transmitting and receiving first messages over and from said medium, each of said cells having a unique cell identification number, all of said first cells having a first group identification number, one of said first cells being programmed to sense a first

condition and to prepare one of said first messages in response to said first condition and another of said first cells being programmed to control a first object in response to said one of said first messages, said first cells communicating with one another over said medium by using one of said first cell's identification numbers and said first group identification number;

a second plurality of programmable cells coupled to said medium for transmitting and receiving second messages over and from said medium, each of said second cells having a unique cell identification number, all of said second cells having a second group identification number, one of said second cells being programmed to sense a second condition and to provide one of said second messages in response to said second condition and another of said second cells being programmed to control a second object in response to said one of said second messages, said second cells communicating with one another over said medium by using one of said second cell's identification numbers and said second group identification numbers;

a third programmable cell coupled to said medium having a unique cell identification number, and having said first group identification number, said third cell for performing one of the functions of sensing or controlling by employing said first messages, said third cell having said second group identification number for purposes of repeating said second messages;

whereby a network for sensing, communicating and controlling is realized.

17. The network defined by claim 16 wherein said first cells, second cells and third cell have a common system identification number.

18. The network defined by claim 17 wherein said first cells, second cells and third cell are each an integrated circuit.

19. The network defined by claim 18 wherein each of said first cells, second cells and third cell includes a processor and an input/output section for coupling said processor to said medium.

21. The network defined by claims 16 or 20 wherein said other of said first cell sends an acknowledgement message in response to said one of said first messages.

22. The network defined by claim 21 wherein said other of said second cells sends an acknowledgement message in response to said one of said second messages.

First Hit Fwd Refs

Generate Collection Print

L14: Entry 2 of 3 File: USPT Mar 7, 2000

DOCUMENT-IDENTIFIER: US 6032857 A
TITLE: Electronic money system

Brief Summary Text (12):
The transaction information details include detailed information about the purchases made with the IC card, such as the names of the commodities purchased, the classification of use and the like and detailed information using transaction information about the electronic money as an index. The detailed information is stored on the IC card and then read by a personal computer or special purpose data processor and the like so that it can be used for management of expenses made with the IC card, such as personal or household expenses.

Detailed Description Text (5):
Within the bank branch system 1, banking teller terminals 12 are provided for accepting payments with the associated card reader/writers 11. The banking teller terminals 12 are connected to the transaction management terminal for electronic money 16 through an internal communication line 13. A value box 15 and a relay computer are connected to transaction management terminal 16. Further, an automated teller machine 14 is connected to terminal 16 through the internal communication line 13.

Detailed Description Text (17):
During the withdrawal of the aforesaid electronic money, the IC card possessed by the individual is connected to an IC card in the value box 15 of the bank branch system 1 via the IC card reader/writer of the banking teller terminal 12, the auto teller machine 14, the personal computer 32 or the IC card telephone 34, by the communication function incorporated in the individual's IC card. Then, the electronic money stored in the IC card 10 in the value box 15 of the bank branch system 1 is stored in the IC card 10 possessed by the individual, under the control of the transaction management terminal for electronic money 16. At this time, the amount stored in the IC card 10 possessed by the individual is subtracted from the balance of the electronic money stored in the IC card 10 in the value box 15 of the bank branch system 1. The withdrawal of the deposit from the individual's account is carried out in a manner similar to that conventionally practiced by banks.

Detailed Description Text (22):
If the customer pays with the IC card in which electronic money is stored, not in cash, the customer inserts the IC card into a card slot of the POS terminal for electronic money 21 or into the IC card reader/writer 11 connected to the normal POS terminal 22. Thus, the IC card of the customer and one of the IC cards in the value box 15 installed in the centre device 24 of the store are connected to each other via the internal communication line 13 and the work station 26, so that the electronic money stored in the IC card of the customer is transferred to the one IC card in the value box 15 installed in the centre device 24 and a receipt is output from the POS terminal to complete the payment transaction for purchasing the commodity. In this case, the electronic money stored in the IC card of the customer is decreased by the amount paid for by the purchase transaction, and this amount is added to the electronic money of the IC card of the store.

First Hit Fwd Refs

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L14: Entry 2 of 3 File: USPT Mar 7, 2000

US-PAT-NO: 6032857
DOCUMENT-IDENTIFIER: US 6032857 A

TITLE: Electronic money system

DATE-ISSUED: March 7, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Kitagawa; Hiroki	Tokyo			JP
Miyamoto; Yo	Fuchu			JP
Furuta; Jun	Kokubunji			JP
Takano; Masaki	Musashino			JP
Matsubara; Takashi	Kodaira			JP
Ohsawa; Takao	Niiza			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hitachi, Ltd.	Tokyo			JP	03

APPL-NO: 08/ 807630 [PALM]
DATE FILED: February 27, 1997

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	8-042792	February 29, 1996

INT-CL: [07] G06 F 17/60

US-CL-ISSUED: 235/379; 902/24
US-CL-CURRENT: 235/379; 902/24

FIELD-OF-SEARCH: 235/379, 235/380

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	5453601	September 1995	Rosen	235/379

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
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542298A	May 1993	EP	
653717A	May 1995	EP	
686947A	December 1995	EP	
4203748A	August 1993	DE	
62-25372	February 1987	JP	
4-233097	August 1992	JP	
7-334587	December 1995	JP	
WO9113411A	September 1991	WO	

OTHER PUBLICATIONS

Mondex Magazine, Launch Issue, Jul., 1995.

ART-UNIT: 286

PRIMARY-EXAMINER: Pitts; Harold I.

ATTY-AGENT-FIRM: Beall Law Offices

ABSTRACT:

An electronic money system has an IC card for electronic money having a memory for maintaining money deposit and money debit information and another memory, such as an EPROM, for storing transaction data, including detailed information of transactions, such as the content of a typical receipt received from a retail store. The transaction information can be used at a later time in a personal computer so that an electronic record of household expenses can be maintained The transaction data that is stored includes the product name, price of the product, quantity of the product purchased and similar details of the transaction. The IC card memory can record the name and telephone number of a retail store where the card has been used or a network address can be recorded in the memory for use by a customer to access electronic direct-mail information by using a PC. Also, a store can determine whether a particular purchase is within a range of average purchases in terms of the number of products being purchased in a transaction and the total cost of the transaction, based on the stored transaction information.

9 Claims, 10 Drawing figures

First Hit Fwd Refs

Generate Collection Print

L13: Entry 21 of 38 File: USPT Mar 28, 2000

US-PAT-NO: 6042002
DOCUMENT-IDENTIFIER: US 6042002 A

TITLE: Holding apparatus for a plurality of IC cards facilitating transactions of electronic money among the IC cards

DATE-ISSUED: March 28, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ohki; Masayuki	Kokubunji			JP
Urushihara; Atsuhiko	Kokubunji			JP
Furuya; Jun	Kokubunji			JP
Itoh; Shigeyuki	Kawasaki			JP
Kitagawa; Hiroki	Tokyo			JP
Oosawa; Takao	Niiza			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Hitachi, Ltd.	Tokyo			JP	03

APPL-NO: 08/ 759806 [PALM]
DATE FILED: December 3, 1996

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	7-320629	December 8, 1995
JP	7-333029	December 21, 1995

INT-CL: [07] G06 F 19/00

US-CL-ISSUED: 235/379; 235/380, 235/382, 902/24
US-CL-CURRENT: 235/379; 235/380, 235/382, 902/24

FIELD-OF-SEARCH: 235/379, 235/381, 235/439, 235/440, 235/441, 235/486, 235/492, 235/382, 902/26, 902/24, 194/200

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3833885	September 1974	Gentile et al.	235/379
☐	3845277	October 1974	Voss et al.	235/379
☐	4087680	May 1978	Mack et al.	235/380
☐	4512453	April 1985	Schuller et al.	194/200
☐	4562341	December 1985	Ohmae et al.	235/379
☐	4598378	July 1986	Giacomo	194/200
☐	4802218	January 1989	Wright et al.	235/492
☐	4906828	March 1990	Halpern	235/379
☐	4977595	December 1990	Ohta et al.	235/379
☐	5209335	May 1993	Shuren et al.	194/200
☐	5318164	June 1994	Barnes et al.	194/200
☐	5434395	July 1995	Storck et al.	235/379
☐	5453601	September 1995	Rosen	235/379
☐	5455409	October 1995	Smith et al.	235/441
☐	5519669	May 1996	Ross et al.	902/6

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3840-624	June 1990	DE	194/200
82201100	January 1982	JP	194/200
403251986	November 1991	JP	
5-94458	April 1993	JP	
6-111080	April 1994	JP	
7-254035	October 1995	JP	

ART-UNIT: 286

PRIMARY-EXAMINER: Lee; Michael G

ASSISTANT-EXAMINER: Dunn; Drew A.

ATTY-AGENT-FIRM: Beall Law Offices

ABSTRACT:

In a value box in an electronic money system with a high reliability which is excellent in usage efficiency and maintenance, a front door and a rear door are provided before and after a main body portion and an indicator is provided to show operating states of a door locking key and a whole value box, particularly, a state in which a trouble or the like has occurred in the value box and a maintenance is necessary is provided for the front door. A communication line for transmitting information regarding power source lines and electronic money for a number of IC card readers/writers provided in the main body is connected to the rear door. The

front door can be opened by hinges. A number of IC card readers/writers are enclosed in the main body portion. IC card inserting slots of IC cards for those IC card readers/writers are arranged and provided in the front surface of the main body portion at two upper and lower stages. An IC card operation indicator is provided in correspondence to each IC card inserting slot.

41 Claims, 14 Drawing figures

First Hit   Fwd Refs

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L13: Entry 21 of 38   File: USPT   Mar 28, 2000

DOCUMENT-IDENTIFIER: US 6042002 A
TITLE: Holding apparatus for a plurality of IC cards facilitating transactions of electronic money among the IC cards

Detailed Description Text (4):
FIG. 1 shows a construction of an electronic money system according to an embodiment. Reference numeral 1 denotes a system in a bank branch; 2 a system in a sales store as a broad meaning incorporating a wholesale and the like (hereinafter, such a system is referred to as a retail store system for simplicity of explanation) 3 a shop of a very small scale of a person or private management (hereinafter, such a shop is referred to as a public user for simplicity of explanation) 4 a system for a vending machine; 5 a computing center for managing each branch of a bank; 6 an electronic money originator; 7 a public telephone line; 10 an IC card constructed, for example, so as to be easily portable in a petty current electronic money holding apparatus (electronic purse); 11 a reader/writer of an externally attached IC card; 12 a banking teller of the branch of the bank; 13 an internal communication line; 14 a cash automatic teller machine; 15 an electronic money holding apparatus (hereinafter, referred to as a value box for simplicity of explanation) showing an embodiment of the invention; 16 an electronic money transaction management terminal for electronic money; and 17 a relay computer for processing information so that the public communication network can be used and for transmitting and receiving. Reference numeral 21 denotes a POS terminal for an electronic money; 22 a POS terminal; 23 a store controller; 24 a center device for collecting management data of the sales store and holding and managing the money; 25 a value control and management system; 26 a workstation; 31 an electronic wallet; 32 a personal computer; 33 a PC card type card reader/writer; 34 an IC card telephone; 41 a built-in type IC card reader/writer; 42 a vending machine; 51 an accounting system host; 52 an external accounting system; and 53 a control terminal of the external accounting system.

Structured Search

Database:

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US Patents Full-Text Database
US OCR Full-Text Database
EPO Abstracts Database
JPO Abstracts Database
Derwent World Patents Index
IBM Technical Disclosure Bulletins

Searchable Index: <none> - All Fields | Not Numeric

Term 1 text:

Operator: AND **Proximity Distance:** 1

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Term 2 text:

Display: 10 **Documents in Display Format:** - **Starting With #:** 1

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Search History

DATE: Thursday, April 29, 2004 Printable Copy Create Case

Set Name side by side	**Query**	**Hit Count**	**Set Name** result set
	DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR		
L14	L13 and data near processor	3	L14
L13	terminal near electronic near money	38	L13
L12	L11 and disconnect	10	L12
L11	L10 and data near processor	39	L11
L10	L9 and (bidirectional or bi-directional) near paths	297	L10
L9	("ic card" or "integrated circuit")	486117	L9
L8	L7 and control near unit	12	L8
L7	L6 and switch	38	L7
L6	L5 and external near processor	70	L6
L5	first near path and second near path	31150	L5
L4	L2 and ("ic card" or "integrated circuit card")	23	L4
L3	L2 and "ic card"	23	L3

L2	L1 and exchang$ near money	37	L2
L1	electronic near purse	739	L1

END OF SEARCH HISTORY

First Hit Fwd Refs

End of Result Set

Generate Collection Print

L14: Entry 20 of 20 File: USPT Apr 17, 1990

US-PAT-NO: 4918690
DOCUMENT-IDENTIFIER: US 4918690 A

TITLE: Network and intelligent cell for providing sensing, bidirectional communications and control

DATE-ISSUED: April 17, 1990

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Markkula, Jr.; Armas C.	Woodside	CA		
Sander; Wendell B.	Los Gatos	CA		
Evan; Shabtai	Saratoga	CA		
Smith; Stephen B.	Scotts Valley	CA		
Twitty; William B.	Santa Cruz	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Echelon Systems Corp.	Los Gatos	CA			02

APPL-NO: 07/ 119330 [PALM]
DATE FILED: November 10, 1987

INT-CL: [04] H04J 3/26

US-CL-ISSUED: 370/94; 370/85, 340/825.52
US-CL-CURRENT: 370/400; 340/825.52

FIELD-OF-SEARCH: 340/825.53, 340/825.52, 340/825.5, 340/825.51, 370/92, 370/94, 370/60, 370/85, 370/100, 371/52

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected Search ALL Clear

PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
3699523	October 1972	Percher	340/825.53
4131881	December 1978	Robinson	340/825.53
4535450	August 1985	Tan	370/94

☐	4594708	June 1986	Servel et al.	370/100
☐	4596025	June 1986	Satoh	370/100
☐	4761646	August 1988	Choquet et al.	340/825.52

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ART-UNIT: 263

PRIMARY-EXAMINER: Olms; Douglas W.

ATTY-AGENT-FIRM: Blakely, Sokoloff, Taylor Zafman

ABSTRACT:

A network for sensing, communcating and controlling including a plurality of cells. Each cell is identified by a permanent, unique identification number. Groups of cells are programmed to perform group functions and are assigned group identification numbers. Communication is performed via a medium using the cell identification numbers and group identification numbers.

24 Claims, 30 Drawing figures

First Hit Fwd Refs

End of Result Set

Generate Collection Print

L14: Entry 20 of 20 File: USPT Apr 17, 1990

DOCUMENT-IDENTIFIER: US 4918690 A
TITLE: Network and intelligent cell for providing sensing, bidirectional communications and control

Brief Summary Text (9):
A network for providing sensing, communications and control is described. A plurality of intelligent cells each of which comprises an integrated circuit having a processor and input/output section are coupled to the network. Each of the programmable cells receives, when manufactured, a unique identification number (48 bits) which remains permanently within the cell. The cells can be coupled to different media such as power lines, twisted pair, radio frequency, infrared ultrasonic, optical coaxial, etc., to form a network.

Detailed Description Text (6):
The arrangement 20 comprises a cell 27 which is connected to the switch 22. The cell is also connected to a transceiver 29 which couples data onto the lines 24 and 25. Power for the transceiver and cell are provided from the power supply 30 which receives power from the lines 24 and 25. For this example, the lines 24 and 25 are ordinary household wiring (e.g., 110VAC) and the power supply 30, a five volt DC supply. The cell 27 is preferably an integrated circuit which is described in more detail beginning with FIG. 10. The transceiver 29 may be any one of many well-known devices for receiving and transmitting digital data and as presently contemplated does not perform any processing on transmitted data. The entire arrangement 20 may be small enough to fit within an ordinary wallmounted electrical box which normally contains an electrical switch.

Detailed Description Text (9):
In FIG. 1, the transceivers 29 and 33 communicate over power lines. The transceivers may communicate with one another in numerous different ways over countless media and at any baud rate. They may, for example, each transmit and receive radio frequency or microwave frequency signals through antennas. The transceivers could be connected to a communications lines, such as an ordinary twisted pair or fiberoptic cable and thus communicate with one another independent of the power lines. Other known communications medium may be employed between the transceivers such as infrared or ultrasonic transmissions. Typical transmission rates are 10K bits per second (KBPS) for power lines. Much higher transmission rates are possible for radio frequency, infrared, twisted pairs, fiberoptic links and other media.

Detailed Description Text (25):
Subchannel: In FIG. 4, a first plurality of cells are shown communicating through a common medium such as a twisted pair 50 (cells are shown as "C", announcers as "A" and listeners as "L"). This (e.g., twisted pair 50) is defined as a subchannel, that is, a set of cells all of which communicate directly with one another over the same medium. A broadcast by any member of the subchannel, such as the cell 49, will be heard by all members of that subchannel over the twisted pair 50.

Detailed Description Text (26):

Channel: A channel comprises two or more subchannels where all the cells communicate using the same medium. In FIG. 4, another plurality of cells are shown coupled to twisted pair 52 forming another subchannel. Assume cells 56 and 57 communicate between one another through a twisted pair 72. They form yet another subchannel. The cells associated with the twisted pairs 50, 52 and 72 comprise a single channel. It is possible that the twisted pairs 50, 52 and 72 are one continuous twisted pair with one subchannel 50 so far apart from the second subchannel 52 that the only communications between subchannels is over the portion of the twisted pair 72 running between cells 56 and 57. In this case the cells 56 and 57 are assigned to be "repeaters" in addition to whatever other function they may serve (e.g., announcer or listener).

Detailed Description Text (39):
Note that even though all the cells are on the same power system of a house, they may not communicate directly with one another. For instance, the announcer 60 may be on one circuit which is only coupled to the listener 65 through long lengths of wire running the length of a home and a low impedance bus bar of a circuit breaker panel. The high frequency communication messages may be sufficiently attenuated through this path to prevent direct communications between cells even though they are physically close to one another.

Detailed Description Text (46):
The cell 65 receives the probe packet through numerous routes, including those which in the diagram appear to be most direct (via cell 62) and those which are longer, for example, via cells 61 and 64. It is assumed that the first probe packet to arrive at cell 65 took the most direct route and is therefore the preferred routing. (Assume that this is via cell 62.) Cell 65 receives a packet which indicates that the probe packet was transmitted by cell 60, repeated by cell 62 and intended for cell 65. The other probe packets received by cell 65 after this first packet are discarded by cell 65.

Detailed Description Text (49):
The group formation described above is shown in FIG. 8 by steps or blocks 68 through 72. Block 68 illustrates the broadcasting of the probe packet (e.g., cell 60 transmits the initial probe packet to all cells). The packet includes the address of a destination cell. As the packet proceeds through the network, the packet and accumulates the ID numbers of those cells repeating the packet (block 69). Block 70 shows the acknowledgement (reply) to the probe packet from the destination cell (e.g., cell 65). This packet returns the ID numbers of the repeaters contained in the first received probe packet. Repeater assignment packets are sent out by the announcer causing each repeater to rebroadcast packets for the group; this is shown by block 71. Finally, as shown by block 72, the destination cell such as cell 65 is designated as a listener.

Detailed Description Text (62):
The first announcer cell that is stimulated via its sensor input (e.g., light switch) controls the group formation process. It chooses a system ID number at random from the range of system ID numbers that have been set aside for preinstallation grouping devices. It chooses a group ID number at random. It then broadcasts the group ID number in a packet that requests a reply from any cells that are members of that group. If the transmitting cell receives any such replies, it chooses another group ID at random. The cell continues this process of selecting a random group ID and testing to see if it is already in use until it finds a group ID that is unused in the system in which it is operating.

Detailed Description Text (64):
If an unassigned cell is a listener, it listens after power-up for a packet. The cell takes the group ID from the first packet it receives and assigns itself to that group. The cell then sends a reply to the announcer cell. This reply is not an acknowledgement only packet; it is a packet that identifies the cell as a listener

in the group and the packet must be acknowledged by the announcer. This assures that all of the listener identification packets will arrive at the announcer even though there will be contention and collisions in the process.

Detailed Description Text (68):
In the above example, the announcer waits to be stimulated via its sensor input. An unassigned announcer waits for its first sensor input stimulation or its first received packet. Of those two events, the event that occurs first determines the subsequent actions of the announcer cell.

Detailed Description Text (69):
If the cell is stimulated first, it controls a group formation process just as in the above example. If the announcer cell receives a group packet first, it joins that group as an announcer. It then sends a packet to the group announcer requesting configuration information about the group (group size, number of announcers, etc.) and the assignment of a group member number.

Detailed Description Text (91):
There is a chance that another announcer cell will be stimulated at the same time. Perhaps someone else throws a light switch or a temperature sensor detects a temperature change. The user may want to verify that the ID received is for the correct cell. To verify that the cell ID is the correct one, the user goes through the announcer stimulation process a second time and verifies that the same results occur.

Detailed Description Text (98):
The link address field is a 48 bit field. When this field is all zeroes the packet is interpreted as a system wide broadcast which is acted upon by all the cells. For instance, a probe packet has an all zero field for the link address. Group addresses are dcontained within the link address. For group addresses the first 38 bits are zero and the remaining 10 bits contain the group address. (The cell ID numbers assigned at the factory mentioned earlier range from 1024 to 2.sup.48 since 2.sup.10 addresses are reserved for groups.) The link address, in some cases, is an individual's cell's address. (For example, when a cell is being assigned the task of repeater or listener.)

Detailed Description Text (113):
First, it should be recalled that as each cell transmits, or retransmits a packet, it calculates a packet CRC field which precedes the end flag. For packets that are repeated, a new CRC is needed since at least the hop count will change, requiring a new packet CRC field for the packet. This CRC field is different from the CRC field discussed in the next paragraph.

Detailed Description Text (125):
Referring to FIG. 10, each cell includes a multiprocessor 100, input/output section 107-110, memory 115 and associated timing circuits shown specifically as oscillator 112, and timing generator 111. Also shown is a voltage pump 116 used with the memory 115. This cell is realized with ordinary integrated circuits. By way of example, the multiprocessor 100 may be fabricated using gate array technology, such as described in U.S. Pat. No. 4,642,487. The preferred embodiment of the cell comprises the use of CMOS technology where the entire cell of FIG. 10 is fabricated on a single silicon substrate as an integrated circuit. (The multiprocessor 100 is sometimes referred to in the singular, even though, as will be described, it is a multiprocessor, specifically four processors.)

Detailed Description Text (133):
The currently preferred embodiment of the processor 100 is shown in FIG. 12 and includes a plurality of registers which communicate with two ALU's 102a and 102b. (Other processor architectures may be used such as one having a "register" based system, as well as other ALU and memory arrangements.) The address ALU 102a

provides addresses for the memory 115 and for accessing the I/O subsections. The data ALU 102b provides data for the memory and I/O section. The memory output in general is coupled to the processor registers through registers 146 to DBUS 223.

Detailed Description Text (134):
The 16-bit ABUS 220 provides one input to the address ALU 102a. The base pointer registers 118, effective address registers 119 and the instruction pointer registers 120 are coupled to this bus. (In the lower righthand corner of the symbols used to designate these registers, there is shown an arrow with a designation "x4". This is used to indicate that, for example, the base pointer register is 4 deep, more specifically, the base pointer register comprises 4 16-bit registers, one for each processor. This is also true for the effective address registers and the instruction pointer registers.) The BBUS 221 provides up to a 12 bit input to the ALU 102a or an 8 bit input to the data ALU 102b through register 142. The 4 deep top of stack registers 122, stack pointer registers 123, return pointer registers 124 and instruction registers 125 are coupled to the BBUS.

Detailed Description Text (140):
Both ALU's 102a and 102b can pass either of their inputs to their output terminals, can increment and can add their inputs. ALU 102b in addition to adding, provides substracting, shifting, sets carry flags 124 (when appropriate), ANDing, ORing, exclusive ORing and one complement arithmetic. The ALU 102b in a single step also can combine the contents of next registers 131 and CRC registers 130 (through paths 222 and 133) and combine it with the contents of one of the top of stack registers 122 to provide the next number used in the CRC calculations. Additionally, ALU 102b performs standard shifting and provides a special nibble feature allowing the lower or higher four bits to be shifted to a higher or lower four bits, respectively. Also, ALU 102b performs a 3-of-6 encoding or decoding described in Section F.

Detailed Description Text (142):
In addition to the basic contact pads additional pads in the presently preferred embodiment will be provided with connections to the ADBUS 224 and the MBUS 225 of FIG. 12. One control contact pad may be provided to disable internal memory. By activating the control contact the internal memory is disable and the data over ADBUS and MBUS is used by the processors. This allows the use of a memory that is external to the cell. It is assumed that the additional contact pads may not be available for use when the cell is in an inexpensive package. These additional contacts may be accessed by wafer probe contacts or from pins in packages that have more than the minimum number of pins.

Detailed Description Text (147):
While in the presently preferred embodiment, the processor operates with the output of the memory being coupled to the DBUS 223 through register 146, the processor could also be implemented with data being coupled directly to the input of ALU 102b. Also, the function performed by some of the other registers, such as the effective address registers 119 can be performed by other registers, although the use of the effective address registers, and for example, the CRC registers, improve the operation of the processor.

Detailed Description Text (151):
The processing system has four processors sharing an address ALU, a data ALU and memory. A basic minor cycle takes four clock cycles for each processor. The ALUs take one clock cycle and the memory takes one clock cycle. The minor cycles for each processor are offset by one clock cycle so that each processor can access memory and ALUs once each basis minor cycle. Since each processor has its own register set it can run independently at its normal speed. The system thus pipelines four processors in parallel.

Detailed Description Text (152):
Each register of FIG. 12 is associated with one of four groups of registers and